Application Note_PNDM12P242A1: Dynamic Characteristic Evaluation Board for PNJ's SiC MOSFET in TO-247-3/-4 Package

About this document

This document is prepared as an application note of how to evaluate the dynamic characteristic for PN Junction Semiconductor（PNJ）'s 1200V/650V SiC MOSFET in TO-247-3/-4 package. The reference board is available for designers to carry out double pulse test of PNJ's SiC MOSFET or driver circuit design based on PNJ's SiC MOSFET.

Demo Product Name: PNDM12P242A1

PN Junction Semiconductor (PNJ) Co., Ltd
PNJ Application Team

The Evaluation and Reference Boards are addressed only to qualified and skilled technical staff, for laboratory usage, and shall be used and managed according to the terms and conditions set forth in this document.

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Contents

About this document 1
Contents 2
1. Introduction 3
2. Board Overview 4
2.1 Structure of Evaluation Board 4
2.2 Physical Dimensions and Pinouts 4
2.3 Details of the two Boards 5
3. Reference Board Description 8
3.1 Mother Board 8
3.1.1 Schematic 8
3.1.2 Layout 9
3.1.3 BOM 11
3.2 Daughter Board for TO247-3 12
3.2.1 Schematic 12
3.2.2 Layout 13
3.2.3 BOM 15
3.3 Daughter Board for TO247-4 16
3.3.1 Schematic 16
3.3.2 Layout 17
3.3.3 BOM 19
4. Double Pulse Test 20
4.1 Double Pulse Test Principle 20
4.2 Start-up Procedure 21
4.3 Test Waveform 22
5 Revision History 23

1. Introduction

The purpose of this evaluation board is to demonstrate the high performance of PNJ' s SiC MOSFETs in TO247-3/-4 package. In order to easily expand the new driver board and replace the device in the test in the future, the design of this evaluation board is divided into one mother board and one driver daughter board, which is shown in Figure.1. The driver daughter board contains half bridge gate drivers, snubber capacitors and optional heatsink, forming a functional half bridge power stage. The mother board includes adjustable voltage isolated power supply, bus capacitors and connectors. The mother board is designed to be used at a bus voltage up to 800V and a pulsed current up to 200A.

This board is designed to make it easy for users to:

1) Use as a layout example of printed circuit board (PCB) and the gate driver reference design for TO247-3/-4 package SiC MOSFET.
2) Evaluate the steady state performance of PNJ' s SiC MOSFET in TO247-3/-4.
3) Evaluate the switching performance and characterize E_{ON} and E_{OFF} losses of SiC MOSFETs.
4) Evaluate the effects of using different values of turn on/turn off gate resistor (Rg) , uni-polar versus bipolar gate, various thermal interface materials and cooling methods.

Fig. 1. PNJ's SiC MOSFET Evaluation Board

2. Board Overview

2.1 Structure of Evaluation Board

Figure 2 shows the structure of the evaluation board. 12V power supply and PWM signal are connected to the mother board (P/N:PNDM12P242A1_M). The clamped inductor and DC source are mounted externally through the connectors in the mother board. The recommended turn-on and turn-off gate voltage are +15V/-3V for PNJ's SiC MOSFET. But, in order to cover most values of the gate voltage of different SiC MOSFETs, both adjustable turn-on and turn-off gate voltage power supply are designed to give the flexibility of gate voltage selection. The driver daughter board (P/N: PNDM12P242A1_D2 for TO247-3, PNDM12P242A1_D1 for TO247-4) is a half bridge power stage consisting of two TO247-3/-4 Package SiC MOSFET (such as P3M06040K3/K4 or P3M12080K3/K4) and independent gate driver IC.

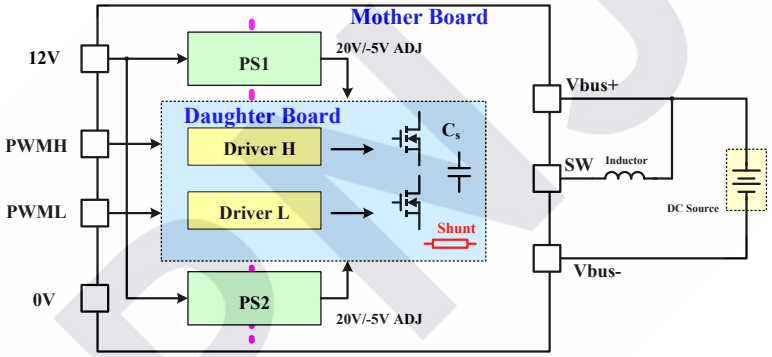

Fig. 2 Structure of Evaluation Board

2.2 Physical Dimensions and Pinouts

Physical dimensions and pinouts of PNJ's PNDM12P242A1 Evaluation Board are shown in Figure 3 and Figure 4. The board has a size of 700mm x100m x 60mm.

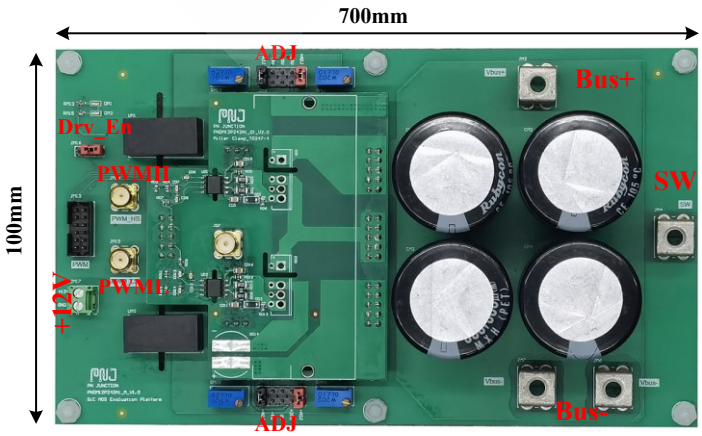

Fig. 3 Top View of PNJ's Evaluation Board

Fig. 4 Front View of PNJ's Evaluation Board

2.3 Details of the two Boards

2.3.1 Mother Board

The mother board includes two sections, the primary supply side on the left and the power circuit as the secondary side on the right. On the primary side, the 12V supply (JM17) and the PWM signals PWM_HS (JM14) and PWM_LS (JM15) are connected from the outside. The Drv_Enable signal (JM16) is used to enable the PWM signals with low level on the left and high level on the right. All these signals can also be connected from the outside through the connector (JM13). The power connectors (JM2, JM4, JM6, JM7) are located on the secondary side. The connectors (JM8, JM10) are designed to adjust the gate voltage. RM12 and RM19 adjusts the turn-off negative voltage (Vee) of the drivers, which ranges from -1.25V to -4V. RM11 and RM18 regulates the turn-on positive voltage (Vcc), which ranges from +10V to +19V. Besides, +20V, 0V and -5V are fixed voltages from isolated DC-DC power supply UM1 and UM2. As can be seen from the figure 5, the driver gate voltage can be configured via two jumpers. Possible configurations are visualized in Table 1.

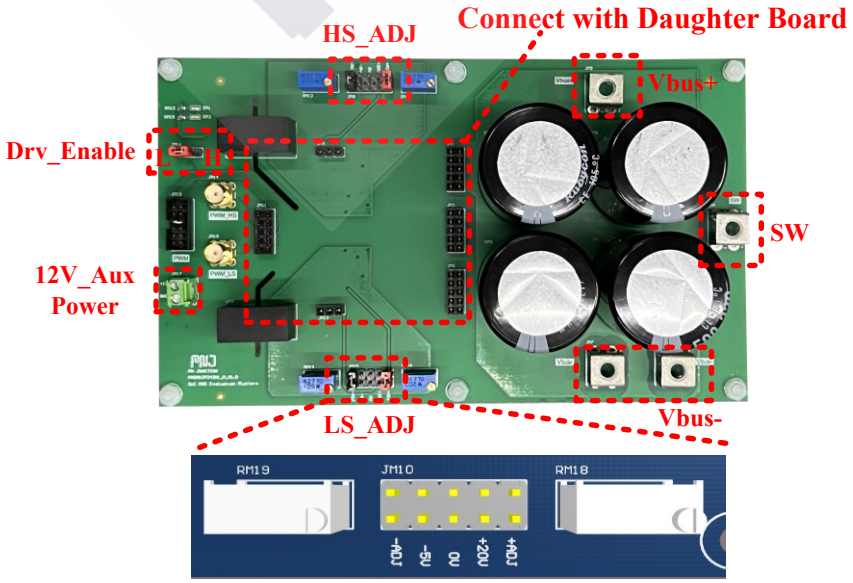

Fig.5 Top View of the Mother Board

Tab.1 Possible Configurations for gate voltage

+20V	0V	+ADJ	-5V	-ADJ
●	●			
●			●	
●				●
	●	●		
		●	●	
		●		●

2.3.2 Driver Daughter Board

Figure 6 displays the function of the driver daughter board of TO247-3 and TO247-4 with Ti 's high transient (dv/dt) immunity driver IC UCC5350MC with miller clamp. The logic power supply 5V and PWM signals are connected to the driver board through the left connector (JD2). The high and low side gate driver power supplys are connected to JD4 and JD6. The signal details of the connectors are shown in Figure 6 (a) of driver board for TO247-4 and figure 6 (b) of driver board for TO247-3. When the Drv_Enable Pin of JD2 brought low, the PWM signals are enabled to perform in normal operating mode. The turn off resistor RD1,RD8 are 5.1Ω and the turn on resistor RD3,RD10 are 8.2 Ω. The suggested driver resistors are between 3Ω to 8Ω for PNJ' s SiC device due to the turn off current and actual PCB Layout. The turn on and off resistors can be 2-3Ω when the voltage spike is smaller than 0.85*Vn (the rated voltage of the device) and make sure the driver ring is not serious.

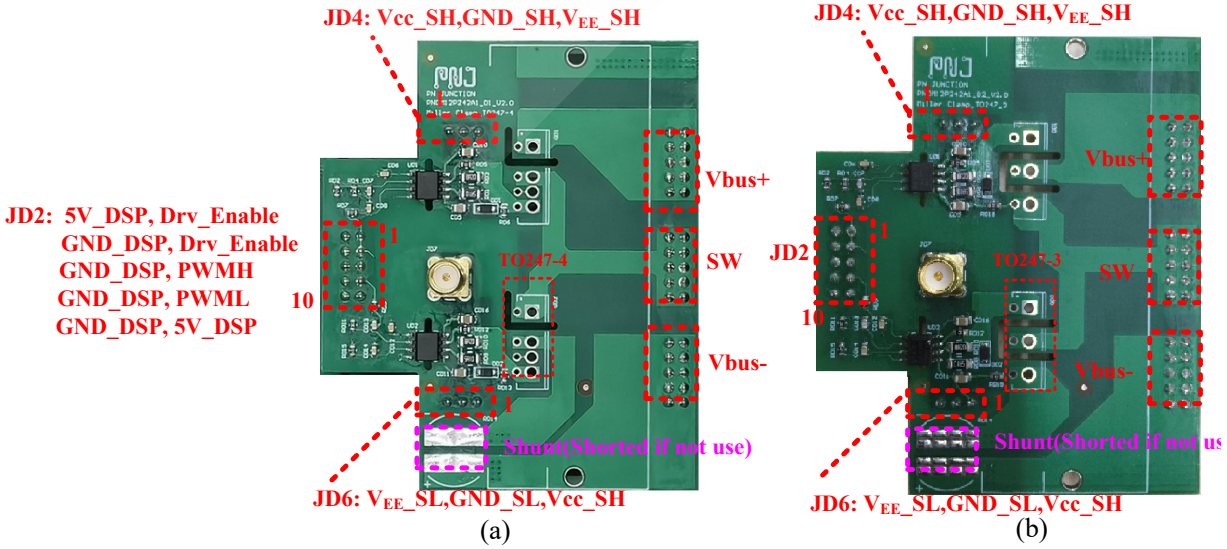

Fig.6 Top View of the Driver Daughter Board for TO247-4 and TO247-3

There are many test points on the driver daughter board, which makes it convenient for user to capture critical waveforms such as drain to source voltage (Vds), gate to source voltage (Vgs) and drain current (Id). It is critical to make these measurements as close as possible to the device pins. As can be seen in figure.7, the test points TP1-TP7 are used for testing the voltage of TO247-3/-4 package MOSFET. The SMA connector JD7 located in the mid of the board is used for monitoring the Vgs of the low side device.

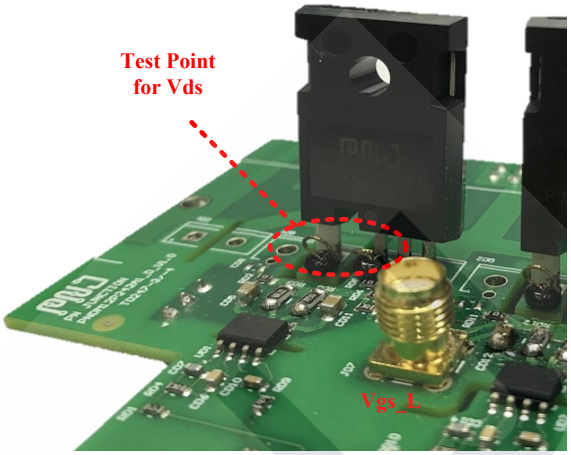

Fig.7 Test point for test Vds and Vgs

In order to test the high speed current of SiC MOSFET in double pulse test, high bandwidth current viewing resistor from T&M Research (P/N: SDN-414-05) is suggested as shown in figure 8. The current viewing resistor from T&M Research has a resistance of 5mΩ; therefore, it is compatible with most oscilloscopes whose probe attenuation can be set to 200X (50Ω input). If the user does not use a current viewing resistor to sense current, then a short jumper must be populated at RD19. RD19 affects the power loop inductance and its inductance should be kept as low as possible. A copper foil or jumper with low inductance is suggested.

Fig.8 Coaxial Shunt for testing Id: SND414-05

3. Reference Board Description

3.1 Mother Board

3.1.1 Schematic

The schematic of the mother board is shown in Figure 9 and Figure 10 .

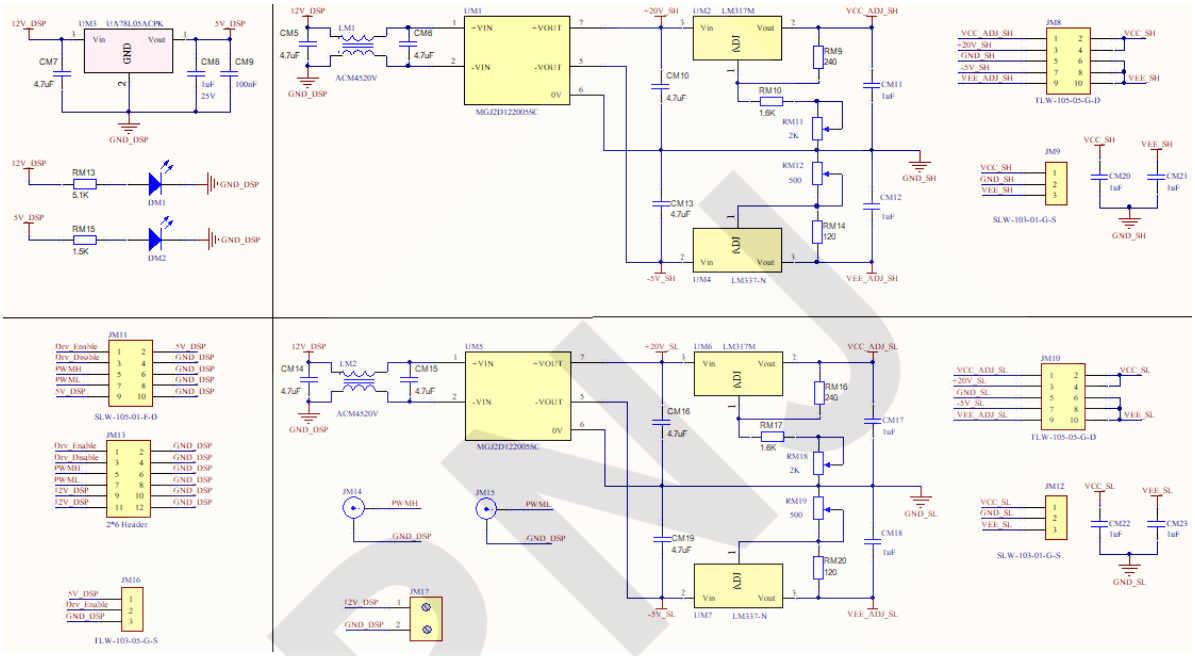

Fig.9 Schematic I of PNJ's mother board

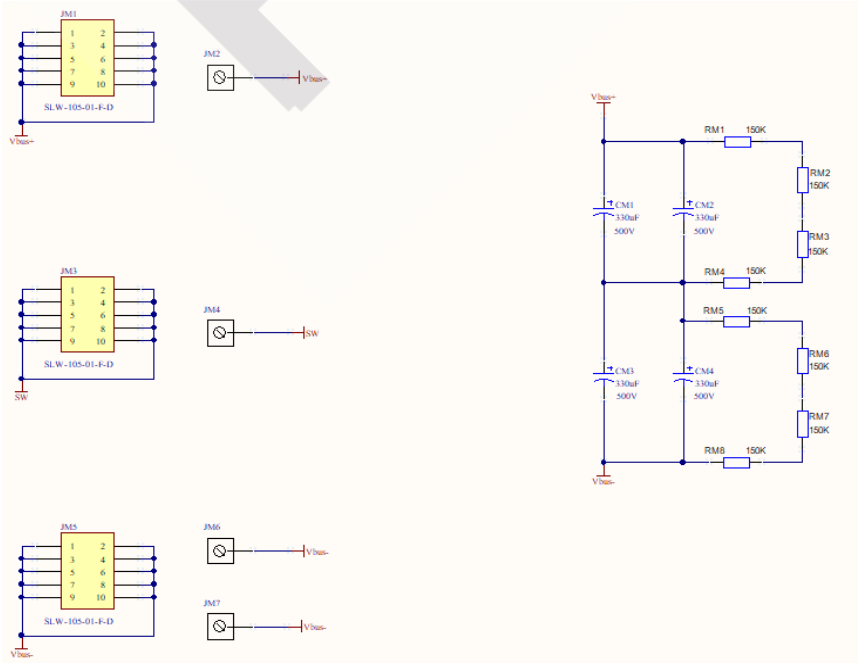

Fig.10 Schematic II of PNJ's Mother board

3.1.2 Layout

The layout of the mother board is shown in Figure 11-Figure 14.

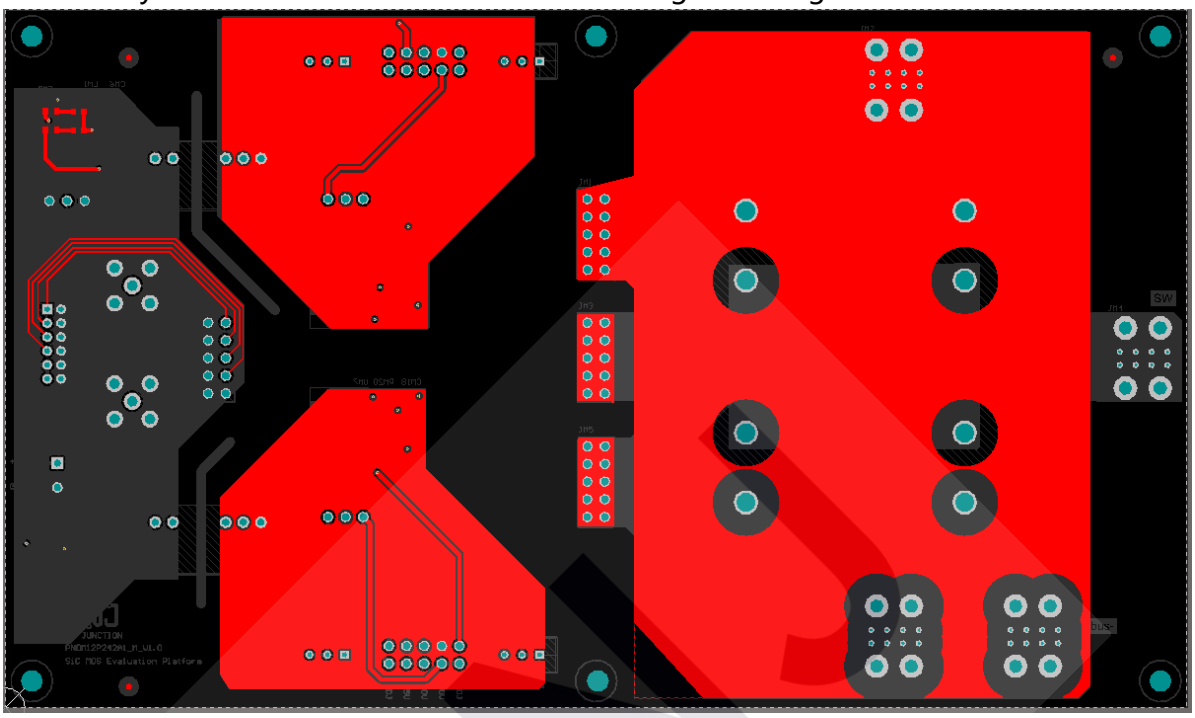

Fig.11 Top layer of the PCB

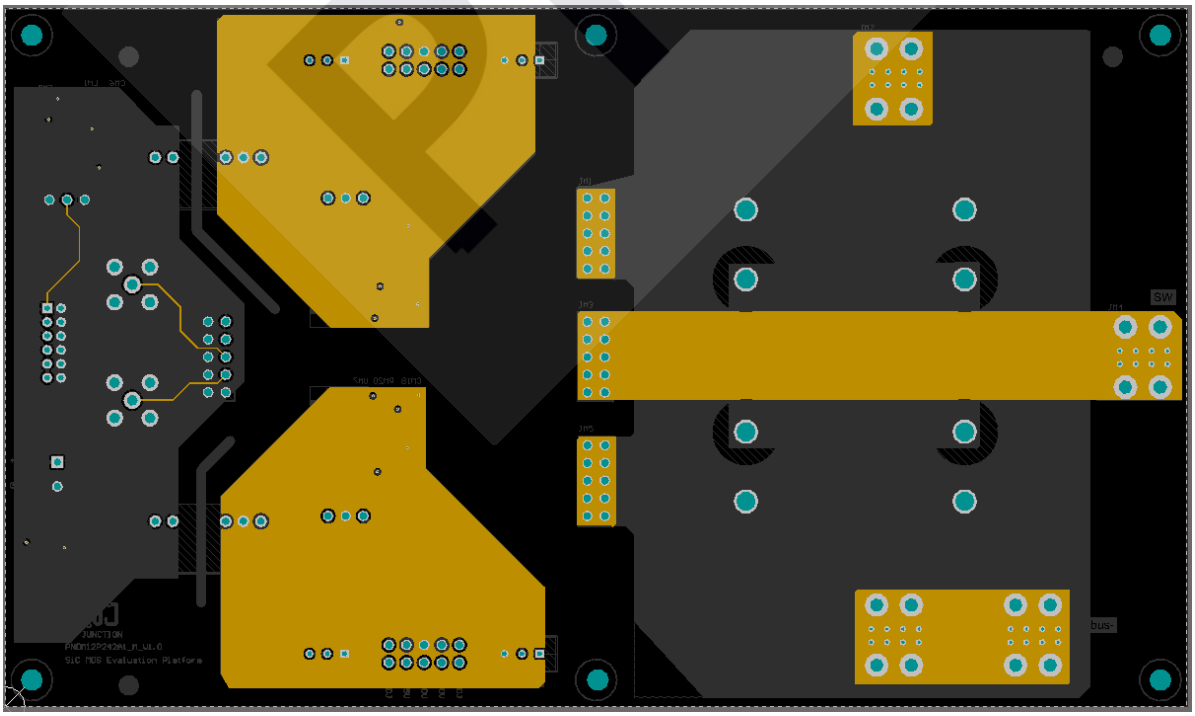

Fig.12 The first mid layer of the PCB

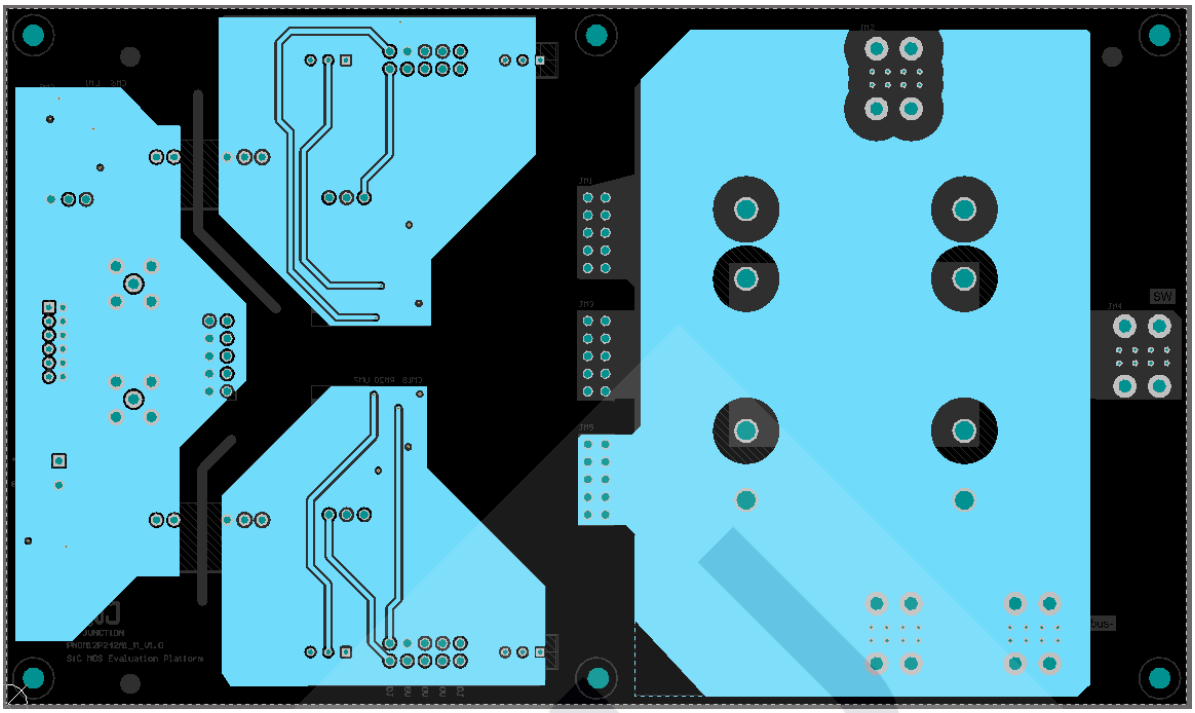

Fig.13 The second mid layer of the PCB

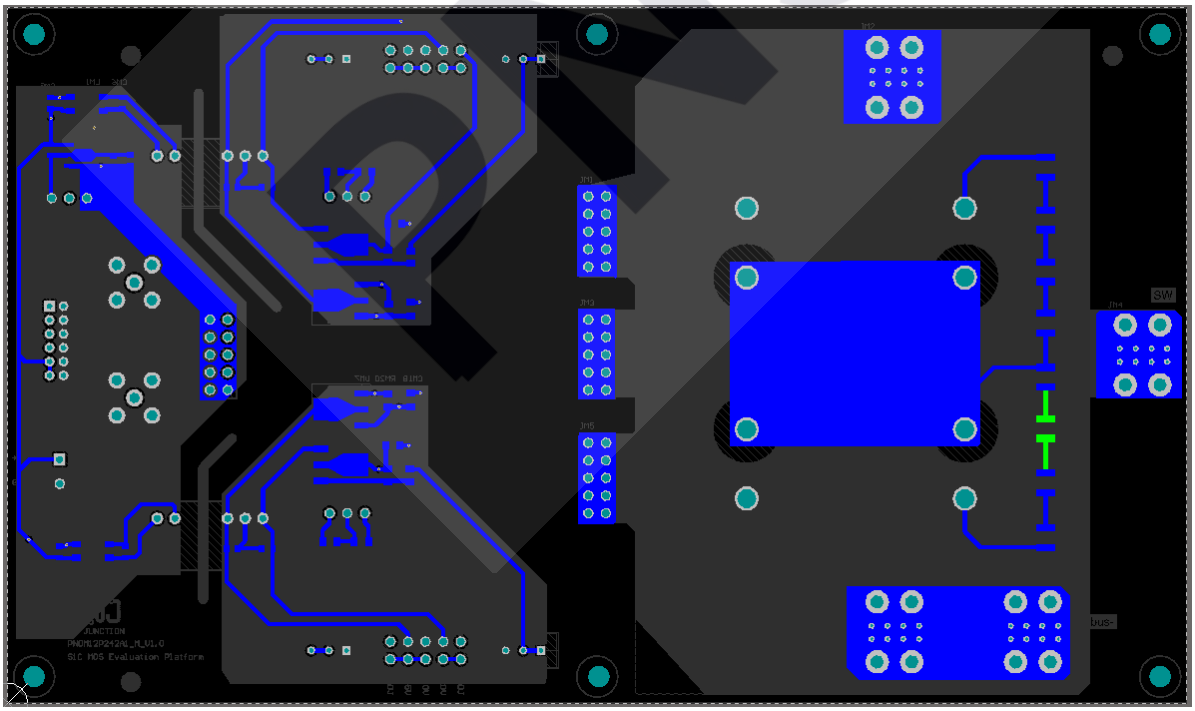

Fig.14 Bottom layer of the PCB

3.1.3 BOM

The BOM list of all components used for the mother board is shown in Tab 2.

Tab.2 The Bill of Material of PNDM12P242A1_M Board

Designator	Description	Manufacturer P/N	Manufacturer	Quantity
CM1, CM2, CM3, CM4	E_Capacitor,330uF/500V,3050mm	500MXH330MEFCSN30X50	Rubycon	4
RM11, RM18	VAR RES 2k Ohm 10% 1/2W 3296W_H10	3296W-1-202LF	Bourns	2
RM12, RM19	VAR RES 500 Ohm 10% 1/2W 3296W_H10	3296W-1-501LF	Bourns	2
CM8	CFCAP X7R S 1μF 25V 0603_H9 belt	06033C105KAT2A	AVX	1
CM9	CFCAP X7R S 100nF 50V 0603_H9 belt	06035C104K4T2A	AVX	1
CM11, CM12, CM17, CM18, CM20, CM21, CM22, CM23	CFCAP X7R S 1μF 25V 0805_H14 belt	08053C105K4T2A	AVX	8
JM2, JM4, JM6, JM7	M4 SCREW MNT TERMINAL,15A	8174	Keystone Electronics	4
JM13	2.00mm Pitch 2*6 125V/2A, Through Hole Connector	87831-1220	Molex	1
JM17	Pitch_3.50 mm _ 2 pins，350VAC/10A	691214110002S	Wurth Elektronik	1
RM15	RES SMD 1.5K 1% 1/10W 0603_H6	AC0603FR-071K5L	Yageo	1
RM13	RES SMD 5.1K 1% 1/10W 0603_H6	AC0603FR-075K1L	Yageo	1
LM1, LM2	Common chock_230R@100MHZ,1.5A/50V,ACM4520V	ACM4520V-231-2P-T00	TDK	2
CM5, CM6, CM7, CM10, CM13, CM14, CM15, CM16, CM19	MLCC - SMD/SMT 0603 25Vdc 4.7uF X5R 10%	GRT188R61E475KE13D	Murata	9
DM1, DM2	LED S green If=20mA,VF=2.2V,LG L29K-G2J1-24-Z	LG L29K-G2J1-24-Z	OSRAM Opto Semiconductors	2
UM2, UM6	IC ADJ REG LINEAR 1.25V~37V 500mA,SOT-223	LM317MQDCYR	Texas Instruments	2
UM4, UM7	IC ADJ REG LINEAR -1.25V~-37V,1.5A, SOT-223	LM337IMP/NOPB	Texas Instruments	2
UM1, UM5	Isolated 2W DC-DC Converters,12-20/-5V	MGJ2D122005SC	Murata	2
RM10, RM17	RES SMD 1.6K OHM 1% 1/8W 0805_H6	RC0805FR-071K6L	Yageo	2
RM14, RM20	RES SMD 120OHM 1% 1/8W 0805_H6	RC0805FR-07120RL	Yageo	2
RM9, RM16	RES SMD 240 OHM 1% 1/8W 0805_H6	RC0805FR-07240RL	Yageo	2
RM1, RM2, RM3, RM4, RM5, RM6, RM7, RM8	RES SMD 150K Ohms 1% 1/2W 1210_H6	RC1210FR-07150KL	Yageo	8
JM9, JM12	2.54mm Pitch 1*3, 300V/5.2A, Through Hole Male Connector	SLW-103-01-G-S	Samtec	2
JM1, JM3, JM5, JM11	2.54mm Pitch 2*5, 300V/5.2A, Through Hole Male Connector	SLW-105-01-F-D	Samtec	4
JM14, JM15	SMA Straight Connector	SMA-J-P-H-ST-TH1	Samtec	2
JM16	2.54mm Pitch 1*3, 300V/5.2A, Through Hole Connector	TLW-103-05-G-S	Samtec	1
JM8, JM10	2.54mm Pitch 2*5, 300V/5.2A, Through Hole Connector	TLW-105-05-G-D	Samtec	2
UM3	IC REG LINEAR 5V 100MA SOT89-3	UA78L05ACPK	Texas Instruments	1

3.2 Daughter Board for TO247-3

3.2.1 Schematic

The schematic of the drive daughter board for TO247-3 is shown in Figure 15.

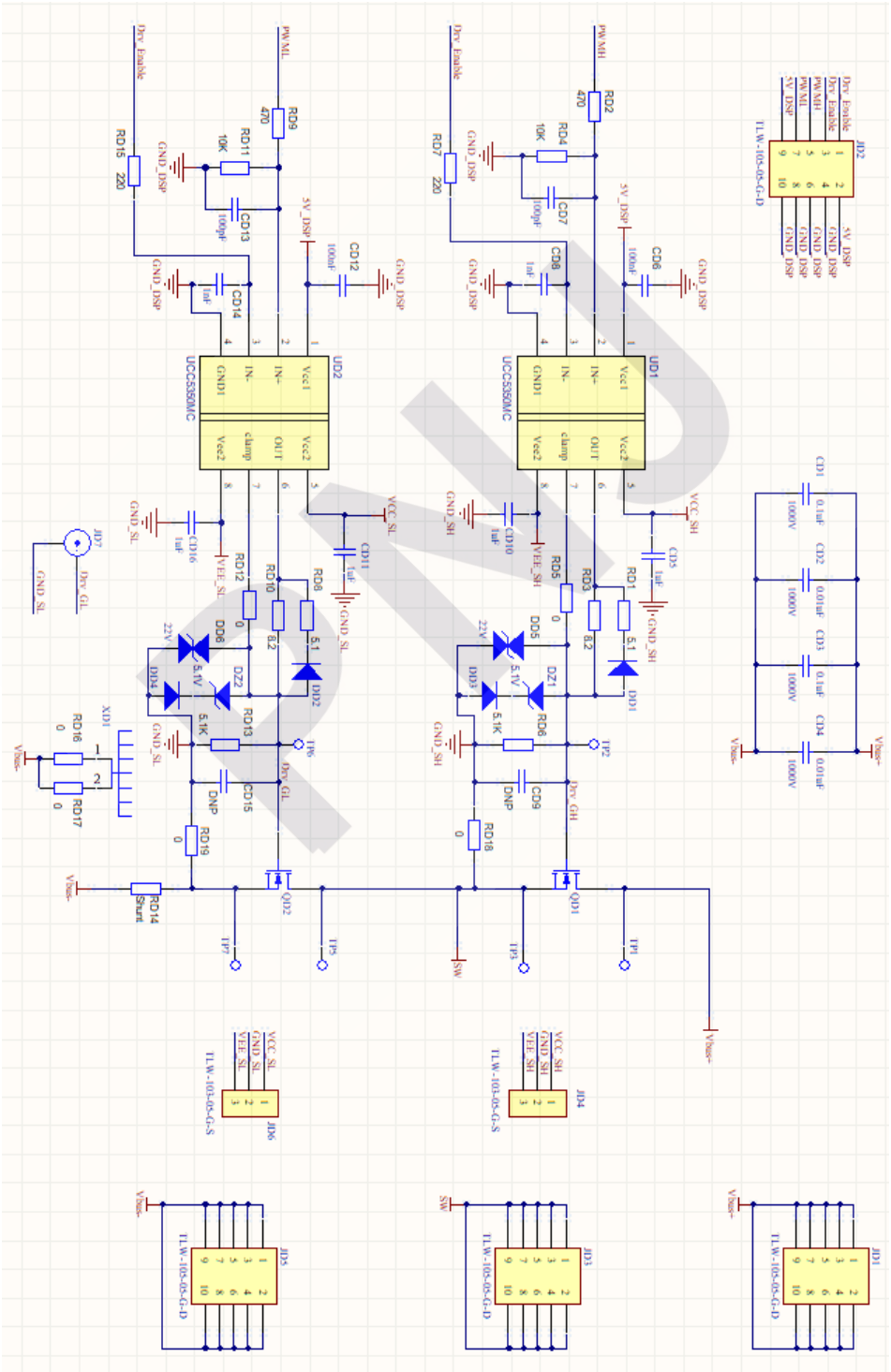

Fig.15 Schematic of PNJ's driver daughter board for TO247-3

3.2.2 Layout

The layout of the daughter board for TO247-3 is shown in Figure 16-Figure 19.

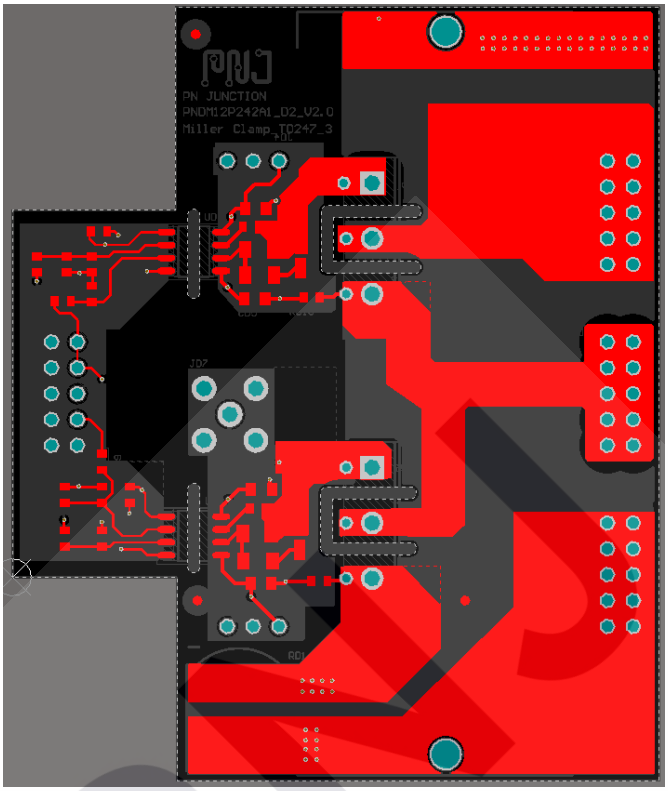

Fig.16 Top layer of the PCB

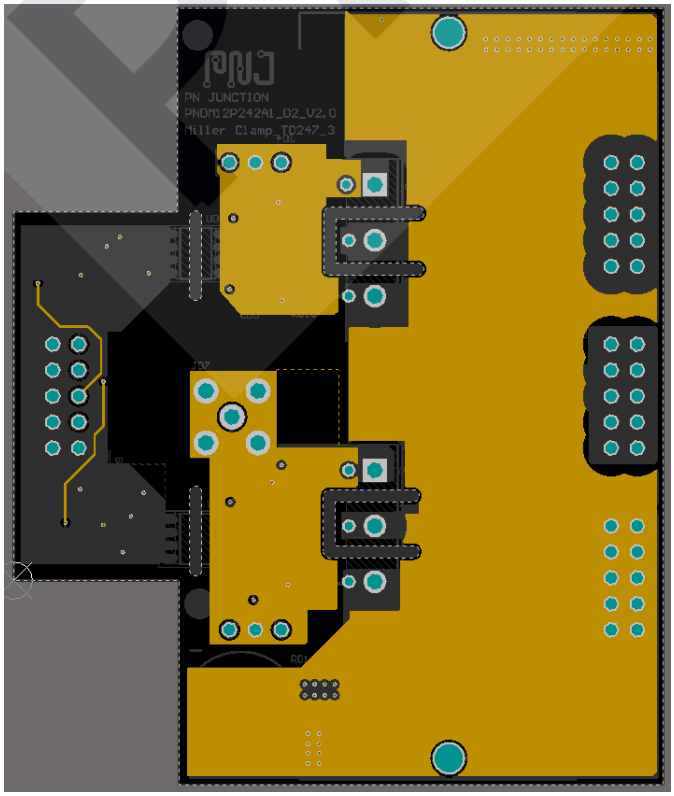

Fig.17 The first mid layer of the PCB

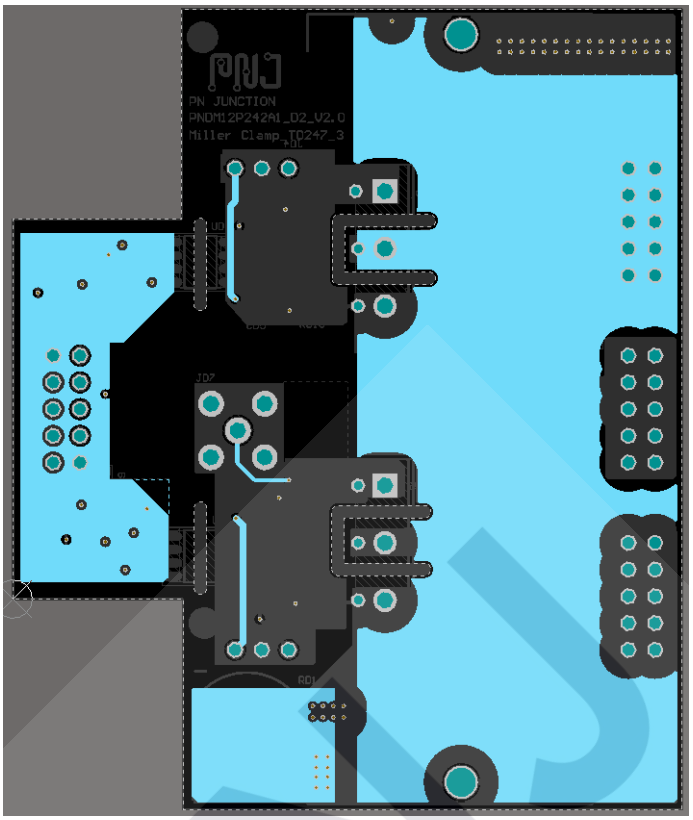

Fig.18 The second mid layer of the PCB

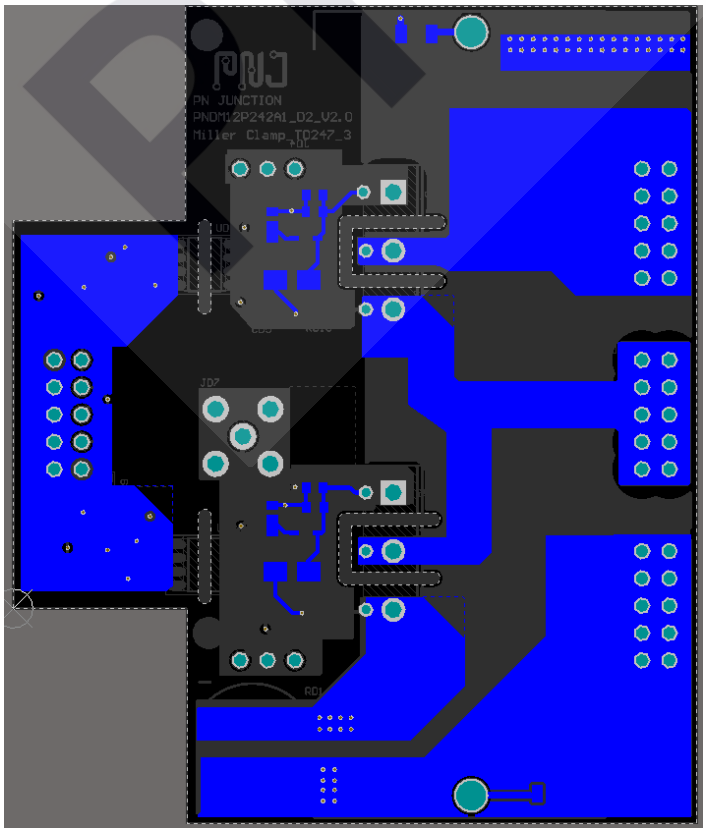

Fig.19 Bottom layer of the PCB

3.2.3 BOM

The BOM list of all components used for the daughter board for TO247-3 is shown in Tab 3.

Tab.3 Bill of Material of PNDM12P242A1_D2 Board

Designator	Description	Manufacturer P/N	Manufacturer	Quantity
CD7, CD13	CAP C0G S 100pF 100V 0603_H09	06035A101J4T2A	AVX	2
CD8, CD14	CFCAP X7R S 1nF 50V 0603_H9 belt	06035C102K4T2A	AVX	2
CD9, CD15	DNP	-	-	2
CD6, CD12	CFCAP X7R S 100nF 50V 0603_H9 belt	06035C104K4T2A	AVX	2
CD5, CD10, CD11, CD16	CFCAP X7R S 1μF 25V 0805_H14 belt	08053C105K4T2A	AVX	4
RD7, RD15	RES S 220.Ohm 1.% 0603_H6 belt	AC0603FR-07220RL	Yageo	2
RD2, RD9	RES SMD 470 OHM 1% 1/10W 0603_H6	AC0603FR-07470RL	Yageo	2
DZ1, DZ2	Z-DIO S 5.1V.BZX84J-B5V1 belt	BZX84J-B5V1,115	Nexperia	2
CD2, CD4	0.01μF ±10% 1000 Ceramic Capacitor X7R 1812_H17	C1812C103KDRACTU	KEMET	2
CD1, CD3	0.1μF ±10% 1000 Ceramic Capacitor X7R 1812_H17	C1812V104KDRACTU	KEMET	2
RD6, RD13	RES SMD 5.1K OHM 1% 1/10W 0603_H6	RC0603FR-075K1L	Yageo	2
RD5, RD12, RD18, RD19	RES SMD 0 OHM 1% 1/10W 0603_H6	RC0603FR-130RL	Yageo	4
RD4, RD11	RES SMD 10K OHM 1% 1/10W 0603_H6	RC0603FR-0710KP	Yageo	2
RD16, RD17	RES SMD 0 Ohms 1% 1/4W 1206_H6	RC1206FR-070RL	Yageo	2
RD1, RD8	RES SMD 5.1Ohms 1% 1/4W 1206_H6	RC1206FR-075R1L	Yageo	2
RD3, RD10	RES SMD 8.2 Ohms 1% 1/4W 1206_H6	RC1206FR-078R2L	Yageo	2
DD1, DD2, DD3, DD4	Schottky barrier diode,30V/1A,IFSM=5A,SOD-323HE	RSX101VYM30FH	ROHM	4
JD7	SMA Straight Connector	SMA-J-P-H-ST-TH1	Samtec	1
JD4, JD6	2.54mm Pitch 1*3, 300V/5.2A, Through Hole Connector	TLW-103-05-G-S	Samtec	2
JD1, JD2, JD3, JD5	2.54mm Pitch 2*5, 300V/5.2A, Through Hole Connector	TLW-105-05-G-D	Samtec	4
UD1, UD2	High CMTI 3kV 12V UVLO single isolated driver	UCC5350MCD	Texas Instruments	2
DD5, DD6	Bidirectional TVS	SMAJ22CA	Littlefuse	2

3.3 Daughter Board for TO247-4

3.3.1 Schematic

The schematic of the drive daughter board for TO247-4 is shown in Figure 20.

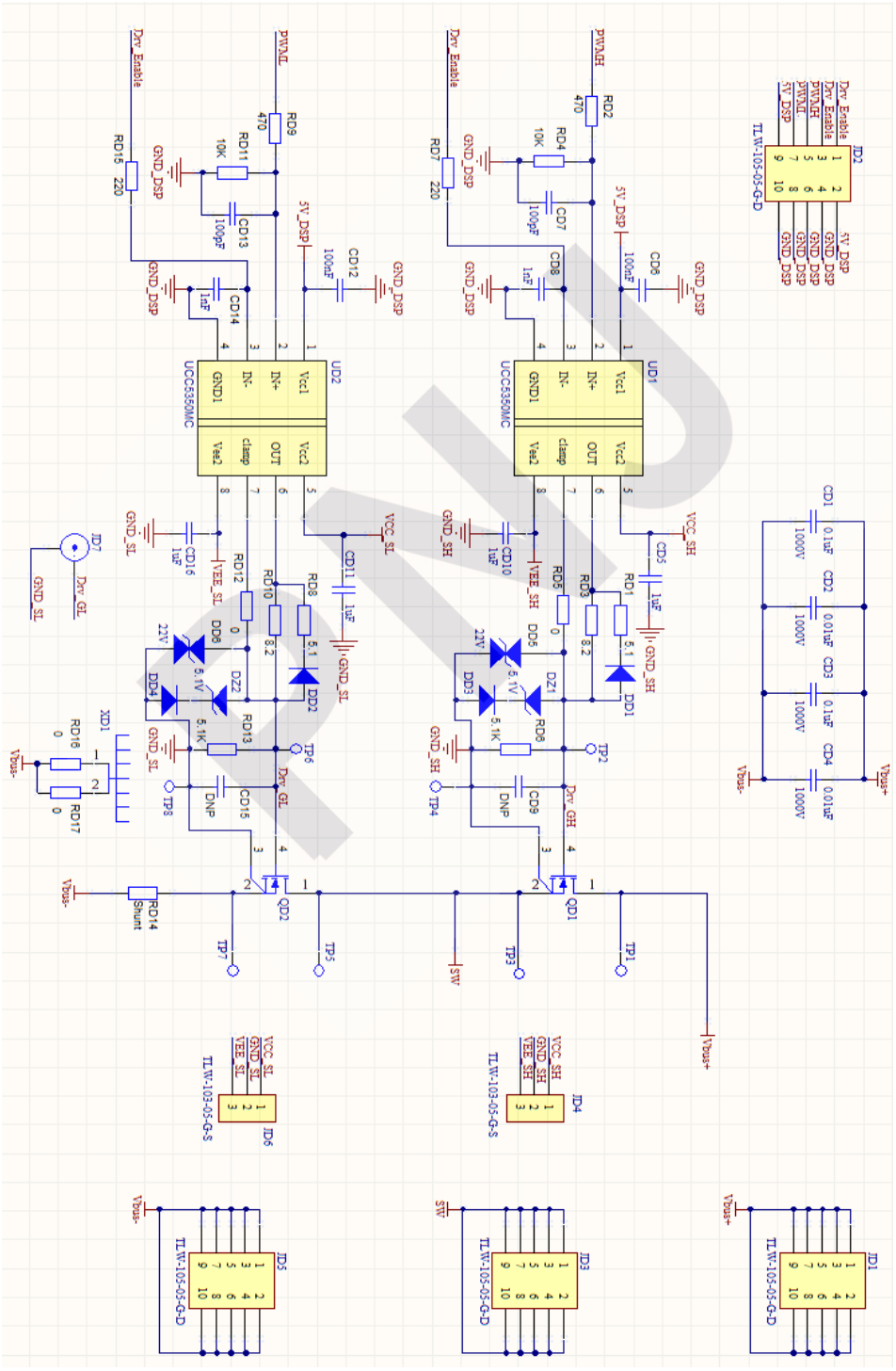

Fig.20 Schematic of PNJ's driver daughter board for TO247-4

3.3.2 Layout

The layout of the daughter board for TO247-4 is shown in Figure 21-Figure 24.

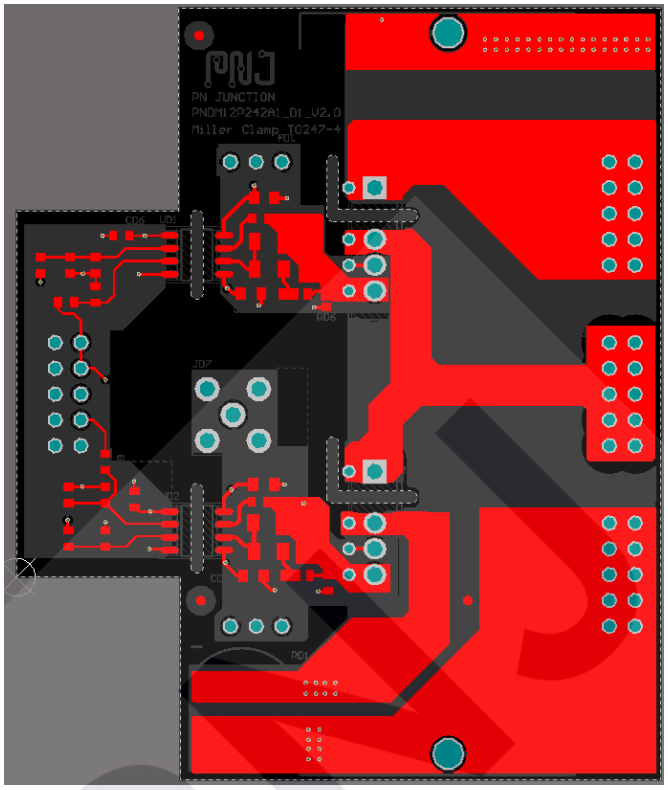

Fig.21 Top layer of the PCB

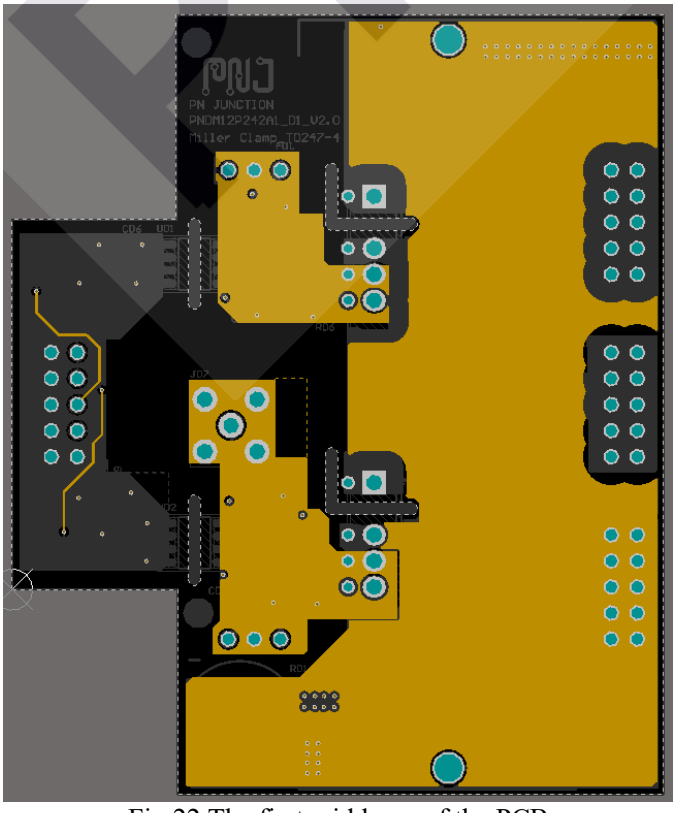

Fig.22 The first mid layer of the PCB

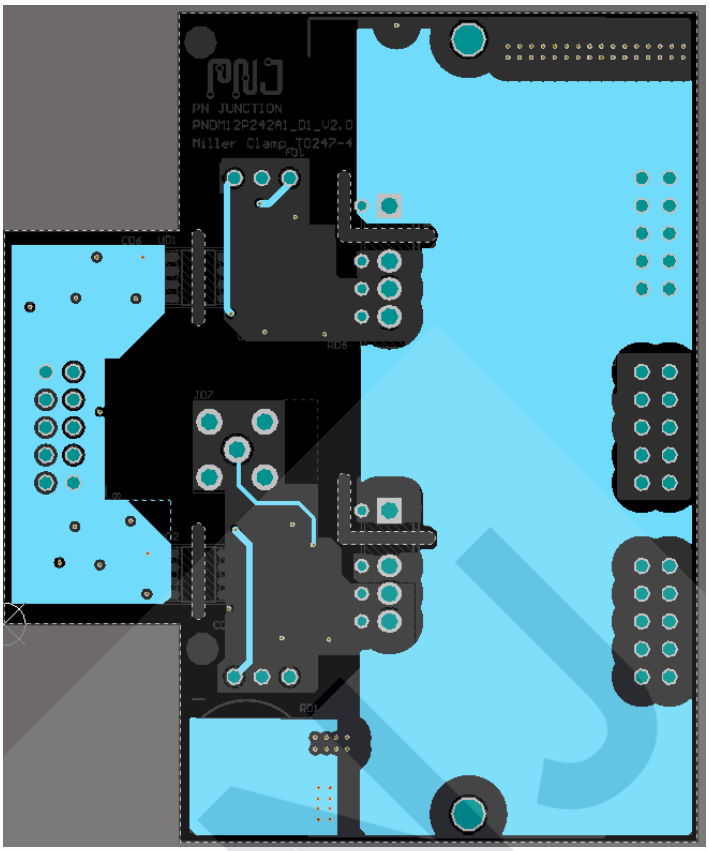

Fig.23 The second mid layer of the PCB

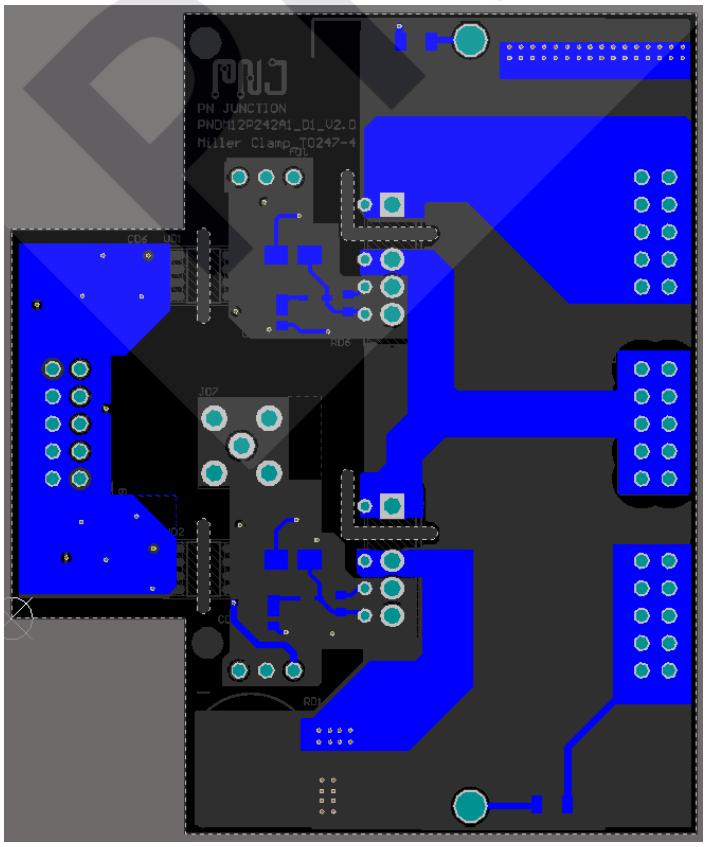

Fig.24 Bottom layer of the PCB

3.3.3 BOM

The BOM list of all components used for the daughter board for TO247-4 is shown in Tab 4.

Tab.4 Bill of Material of PNDM12P242A1_D1 Board

Designator	Description	Manufacturer P/N	Manufacturer	Quantity
CD7, CD13	CAP C0G S 100pF 100V 0603_H09	06035A101J4T2A	AVX	2
CD8, CD14	CFCAP X7R S 1nF 50V 0603_H9 belt	06035C102K4T2A	AVX	2
CD9, CD15	DNP	-	-	2
CD6, CD12	CFCAP X7R S 100nF 50V 0603_H9 belt	06035C104K4T2A	AVX	2
CD5, CD10, CD11, CD16	CFCAP X7R S 1μF 25V 0805_H14 belt	08053C105K4T2A	AVX	4
RD7, RD15	RES S 220.Ohm 1.% 0603_H6 belt	AC0603FR-07220RL	Yageo	2
RD2, RD9	RES SMD 470 OHM 1% 1/10W 0603_H6	AC0603FR-07470RL	Yageo	2
DZ1, DZ2	Z-DIO S 5.1V.BZX84J-B5V1 belt	BZX84J-B5V1,115	Nexperia	2
CD2, CD4	0.01μF ±10% 1000 Ceramic Capacitor X7R 1812_H17	C1812C103KDRACTU	KEMET	2
CD1, CD3	0.1μF ±10% 1000 Ceramic Capacitor X7R 1812_H17	C1812V104KDRACTU	KEMET	2
RD6, RD13	RES SMD 5.1K OHM 1% 1/10W 0603_H6	RC0603FR-075K1L	Yageo	2
RD5, RD12	RES SMD 0 OHM 1% 1/10W 0603_H6	RC0603FR-130RL	Yageo	2
RD4, RD11	RES SMD 10K OHM 1% 1/10W 0603_H6	RC0603FR-0710KP	Yageo	2
RD16, RD17	RES SMD 0 Ohms 1% 1/4W 1206_H6	RC1206FR-070RL	Yageo	2
RD1, RD8	RES SMD 7.5 Ohms 1% 1/4W 1206_H6	RC1206FR-077R5L	Yageo	2
RD3, RD10	RES SMD 8.2 Ohms 1% 1/4W 1206_H6	RC1206FR-078R2L	Yageo	2
DD1, DD2, DD3, DD4	Schottky barrier diode,30V/1A, IFSM=5A,SOD-323HE	RSX101VYM30FH	ROHM	4
JD7	SMA Straight Connector	SMA-J-P-H-ST-TH1	Samtec	1
JD4, JD6	2.54mm Pitch 1*3, 300V/5.2A, Through Hole Connector	TLW-103-05-G-S	Samtec	2
JD1, JD2, JD3, JD5	2.54mm Pitch 2*5, 300V/5.2A, Through Hole Connector	TLW-105-05-G-D	Samtec	4
UD1, UD2	High CMTI 3kV 12V UVLO single isolated driver	UCC5350MCD	Texas Instruments	2
DD5, DD6	Bidirectional TVS	SMAJ22CA	Littlefuse	2

4. Double Pulse Test

4.1 Double Pulse Test Principle

Double pulse test can provide an easy evaluation of device switching performance at high voltage/current without the need of actually running at high power. It can also be used for switching loss (Eon/Eoff) measurement and other switching characterization parameter test.

As can be seen from figure 25 and figure 26, the desired current in the inductive load L is generated from the first pulse (τ_1) , and the Vbus represnts the desired voltage. The first pulse turn-off event leads to a constant current through the body diode of QD1, which can also be replaced by a discrete diode. The second pulse (τ_2) turns on, causing a current overshoot coming from the reverse recovery charge of QD1. Therefore, the end of the first pulse is used for turn-off switching characterization and the beginning of the second pulse is used for turn-on switching characterization.

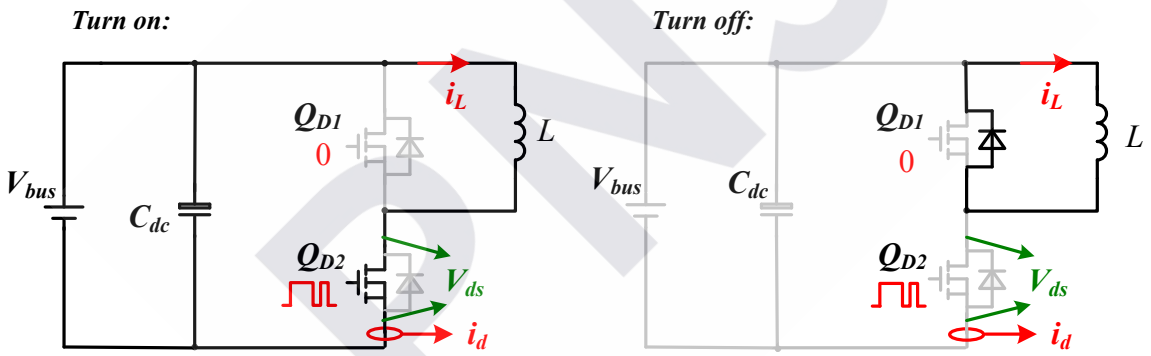

Fig.25 Circuit of double pulse test

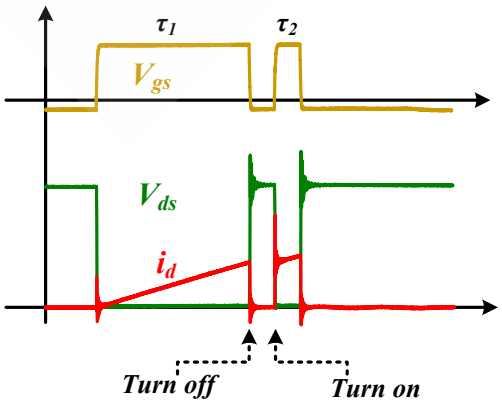

Fig.26 Double pulse test waveforms

4.2 Start-up Procedure

The double pulse signal can be generated by using programmable signal generator or microcontroller/DSP board. As this test involves high switching stress and high current, it is recommended to set the double pulse test gate signal to the single trigger mode or using long repetition period (for example >50-100ms) to avoid the excess of voltage stress during the test.

Following the instructions below to quickly get started with your evaluation of discrete SiC MOSFETs. Equipment and components needed are listed as follows:

- Four-channel oscilloscope with 500MHz bandwidth or higher
- High bandwidth (500MHz or higher) passive probe to test V_{gs}
- High bandwidth (500MHz) high voltage probe (>1200V) to test V_{ds}
- High bandwidth (500MHz) current coaxial shunt to test device current i_d
- AC/DC current probe for inductor current measurement
- 12V DC power supply
- Signal generator capable of creating testing pulses
- High voltage power supply (0-1000VDC) with current limit.
- External power inductor (recommend air core inductor 50-200uH)

Fig. 27 Double pulse test setup example

The double pulse test circuit for the low side switch QD2 testing is shown in figure 25. And the setup is shown in figure 27. The start-up procedure is listed as follows:

1. Solder the DUTs and the coaxial shunt to the driver daughter board.

2. Mount the driver daughter board on the mother board , then set the jumpers for the required supply voltage, the drv_enable signal connector JM16 set to the low level side.
3. Connect the power source (up to 800V), the auxiliary power supply 12V (0.3A) and the clamped inductor. The function generator is connected to JM15 (PWML), the signal of PWMH (the pin 5 of JD2) should be connected to GND.
4. Plug in the desired probes (voltage/current)
5. Edit the double pulse waveform in the programmable signal generator. Use equation $I_L = (V_{bus}*\tau_1)/L$ to calculate the pulse width of the first pulse. Then test the double pulse by oscilloscope.
6. Power-on: Turn on the output of the HV supply. Start with low voltage and slowly ramp the voltage up until it reaches the desired high voltage. During the ramping period, observe the the voltage and current waveforms on the oscilloscope closely.
7. Test: Do double pulse test according to the requirement.
8. Power-off: When the test is completed, ramp down the HV supply voltage to 0V slowly, then turn off the output. After that, turn off the 12V bias supply and signal generator output.

4.3 Test Waveform

Figure 28 shows the hard switching on waveforms of double pulse test at 400V/20A of PNJ' s P3M06040K4 (L=200uH, Rgon=8.2Ω, Rgoff=7.5Ω, Vgs=+15V/-3V)

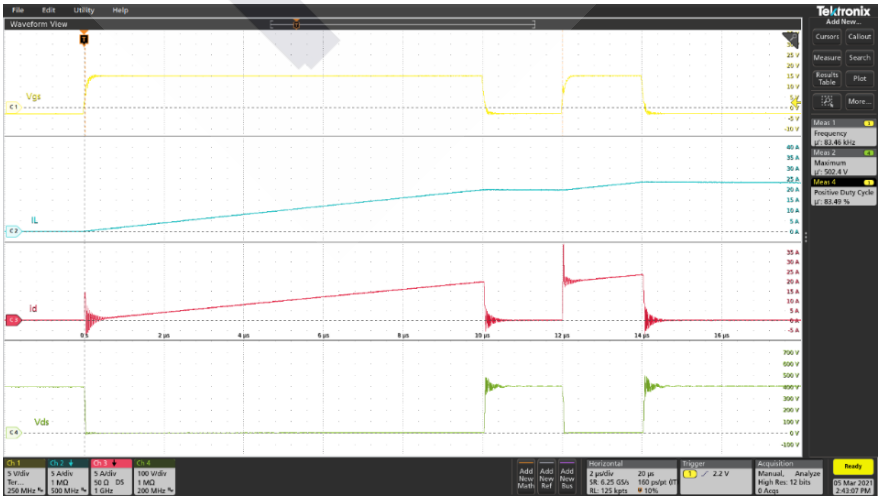

Fig. 28 Double pulse test waveforms of P3M06040K4

The switching energy can be calculated from the measured switching waveform by Psw = Vds*Id. The integral of the Psw during switching period is the measured switching loss.

Reference

[1] P3M12080K3/K4 datasheet, 1200V SiC MOSFET

[2] P3M06040K3/K4 datasheet, 650V SiC MOSFET

[3] UCC5350 datasheet, 5 Amp ISOdriver with High Transient (dV/dt) Immunity

[4] Zheyu Zhang, Ben Guo, Fei (Fred) Wang, etc. Methodology for Wide Band-gap Device Dynamic Characterization, in IEEE Transactions on Power Electronics, vol. 32, no. 12, Dec. 2017, pp. 9307-9318.

5 Revision History

Date	Revision	Description of change
2021.09.10	V1.1	Initial Version